6.5 A WiMedia/MBOA-Compliant CMOS RF Transceiver for UWB

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A completely integrated, WiMedia/MBOA-compliant [1] RF transceiver for Ultra-Wideband (UWB) data communication in the 3 to 5GHz band is presented. It is designed in 0.13µm standard CMOS technology for a single supply voltage of 1.5V. The measured noise figure (NF) of 3.6 to 4.1dB over all three bands is significantly better (2 to 4dB) than existing CMOS [2] or BiCMOS SiGe [3] receive chains, and comparable to the BiCMOS SiGe receiver described in [4]. On the transmit side, an improvement in P_{1dB} of 15dB compared to [2] is achieved, supporting an EVM of -28dB up to -4dBm output power. This output power level is required to support realistic external losses.

The block diagram of the direct conversion transceiver chip is shown in Fig. 6.5.1. The fully differential receiver includes an LNA with high- and low-gain modes and a programmable-gain amplifier (PGA) with 4 gain steps to enable optimum receive performance for different signal strengths and interferer scenarios [5]. The amplifiers are followed by a Gilbert-type down-conversion mixer, which generates quadrature (I and Q) outputs. It is based on a class-AB voltage-to-current converter, a Gilbert Quad, and a load that implements both a current-to-voltage converter and a low-noise filter used to suppress large out-of-band interferers. The position of the filter poles (around 500MHz) can be calibrated digitally by tuning filter capacitors, thus achieving good transition-band and stop-band accuracy in the presence of process variations. The analog I/Q chip interface is driven by an output buffer with a bandwidth of 1GHz to enable characterization of all receive chain impairments.

On the TX side the baseband I/Q analog input signal is converted to a current by a highly linear voltage-to-current converter and fed into Gilbert-type folded upconverting mixers. To reduce the LO leakage caused by dc offset in the mixer stage, a compensation DAC is added and controlled by a serial interface bus. The differential output signal of the mixer is converted to single ended, followed by a programmable gain stage and an integrated 3-stage power amplifier (PA). The 3 required coils in the PA are realized by stacked inductors. Gain-switching is implemented by a capacitive divider with a switchable divider ratio, yielding a variable gain range of 30dB with a resolution of 1dB for high-gain settings. A power detector followed by an ADC with 6b resolution is implemented to measure the output voltage of the PA. Taking into account some back-off due to external losses, antenna and impedance mismatch, this scheme enables cost-efficient control of the actual output power to fulfill TX emission-mask requirements without external components.

Figure 6.5.2 shows the block diagram of the LO generation. To generate the three required LO frequencies of 3.432, 3.960 and 4.488GHz with minimal transition time when hopping, an open-loop topology is required. The principle idea is to add or subtract a low frequency (±264MHz or -792MHz) from a fixed frequency of 4.224GHz. The proposed implementation includes a phase locked loop (PLL), two single-sideband (SSB) mixers (for I and Q channels), and a direct digital synthesizer (DDS) approach for generating the low frequencies. The advantage of this approach is that there is only one SSB mixer stage within the LO generation chain, which eases control of all unwanted spurs generated by the chip. Using the DDS approach the inherent harmonics of the LF signal are much lower than if the LF signal was generated by divider chains or logic operations.

The reference clock is fed to a PLL locking an integrated LC-VCO to 8.448GHz. This frequency is divided by 2 to generate I/Q signals at 4224MHz. Two current-steering 4b DACs running at a sample rate of 4.224GHz generate the three frequencies of ±264MHz and -792MHz. This sample rate was chosen carefully to avoid additional generation of spurs. The sinusoidal I/Q waveforms are stored in ROM lookup tables, which can be selected via the hop control commands.

The transceiver is completed by bandgap-based biasing and a high-speed control interface. The latter is required for real-time update of gain and hopping settings. It is implemented with low-voltage differential signals running at 264Mb/s to fulfill the requirements of high control-speed and low noise-coupling from the interface to the RF part. Figure 6.5.3 shows a micrograph of the chip, which is packaged in a low-cost very thin profile quad flatpack no-lead (VQFN) plastic package with 48 pins. It is fabricated on a 0.13µm standard digital CMOS technology with 1-poly 6-layer copper metal stack and MiM-Capacitors used as the only RF add-on feature.

The transmitter is tested with an OFDM WiMedia/MBOA-compliant signal [1]. On the left side of Fig. 6.5.4 the constellation diagram at the power amplifier output for band 1 is shown at an output power of -7dBm. The corresponding measured EVM is -28dB. For the bands 2 and 3 the measured EVMs are -27.5 and -27dB, respectively. On the right side of Fig. 6.5.4 the EVM in band 1 is shown for varying output power. For large output power levels when the PA is approaching its compression region the EVM degrades. At a power close to 0dBm, the transmitter still meets the required EVM of -20dB [1].

Figure 6.5.5 shows the spectrum at the PA output when operating in time-frequency interleaved (TFI) mode [1], hopping between all 3 bands. The resolution bandwidth of the spectrum analyzer is set to 1MHz as recommended in [6]. The two graphs show the spectrum with power level set close to -41.3dBm/MHz, and with and without external bandpass filter (TDK DEA453960BT). When the filter is used, all spurs are well below -30dBc.

The measured conversion gain and NF of the receiver for all 3 bands are shown in Fig. 6.5.6. The maximum gain and the minimum NF are 37.8dB and 3.6dB respectively. The NF increases to 4.1dB in band 3. The gain variations over the entire baseband frequency range and across all UWB Mode-1 bands are less than 1dB. At low (high) gain setting the IIP3 is +2dBm (-22dBm).

The phase noise of the LO generation is characterized at the TX output. From 100Hz to 100MHz offset the integrated jitter is below $1.2ps_{rms}$ for all three bands, which corresponds to an EVM level of -29.5dBc for band 3. The measured hopping time of the LO generation and receive chain is 2ns, which is well below the required 9.5ns described in [1] and is mainly limited by the filter pole of the mixer output stage. The performance of the UWB RF transceiver is summarized in Fig. 6.5.7.

References:

[1] A. Batra et al., "Multiband OFDM Physical Layer Specification," http://www.multibandofdm.org, Release 1.0, Jan., 2005.
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[4] A. Ismail and A. Abidi, "A 3.1 to 8.2 GHz Direct Conversion Receiver for MB-OFDM UWB Communications," *ISSCC Dig. Tech.Papers*, pp. 208-209, Feb., 2005.
[5] R. Salerno et al., "ESD-protected CMOS 3-5 GHz Wideband LNA+PGA Design for UWB," *Proc. ESSCIRC*, pp. 219-222, Sept., 2005.
[6] http://www.fcc.gov/Bureaus/Engineering_Technology/Orders/2002/fcc02048.pdf, Feb., 2002.

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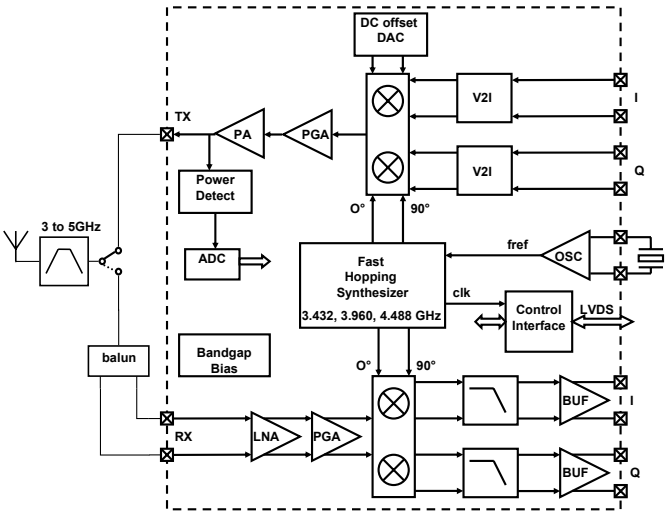

Figure 6.5.1 UWB transceiver block diagram.

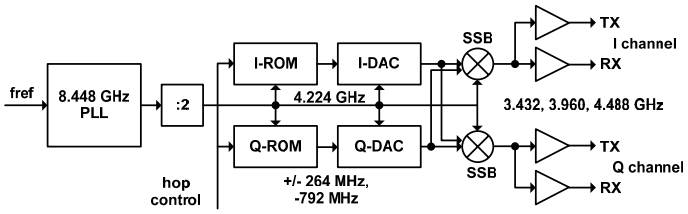

Figure 6.5.2: LO generation block diagram.

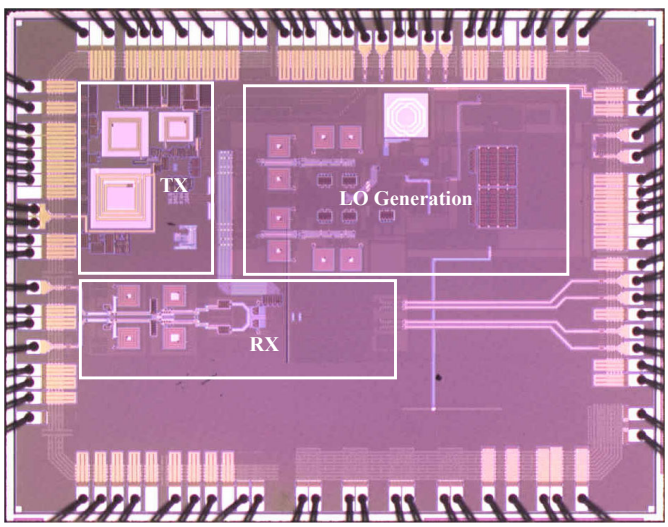

Figure 6.5.3 Chip micrograph.

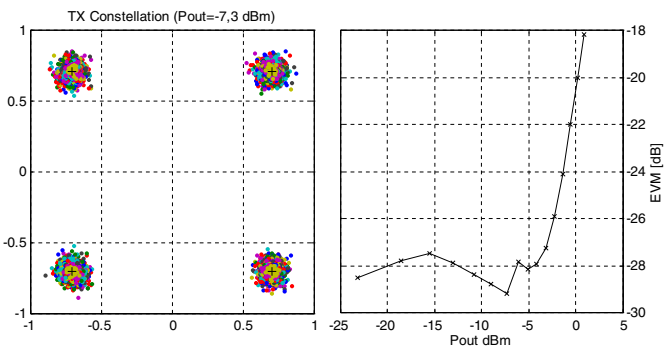

Figure 6.5.4: Measured TX constellation and EVM versus Pout.

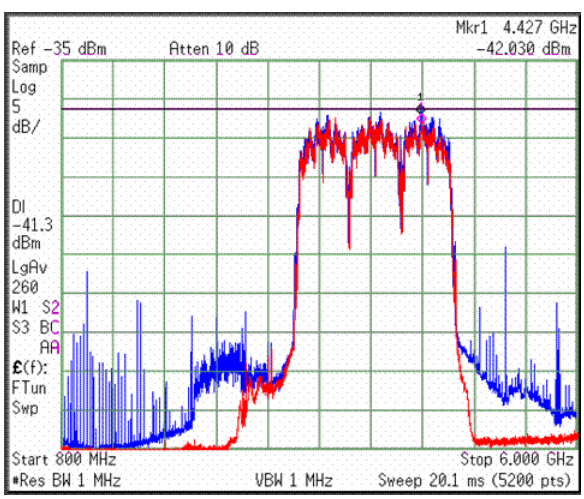

Figure 6.5.5: Measured TX spectrum in TFI mode.

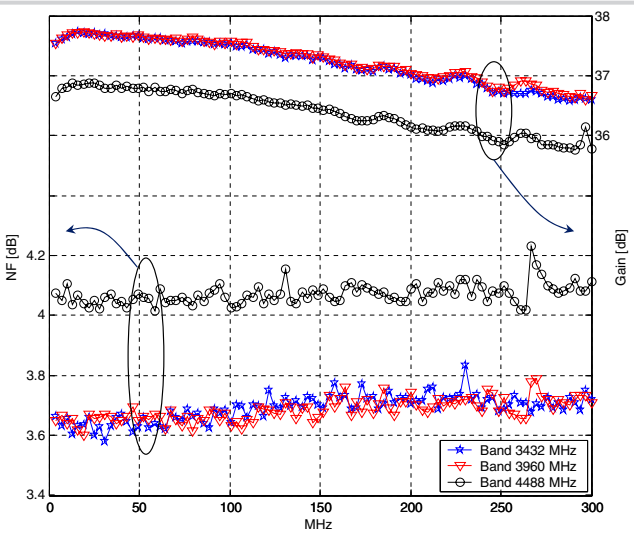

Figure 6.5.6: Measured conversion gain and NF versus baseband frequency over all three bands.

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Parameter	Condition	Value	Unit
RX NF	High gain, band 1 / 2 / 3	3.6 / 3.7 / 4.1	dB
RX gain	High gain, band 1 / 2 / 3	+37 / 37 / 36	dB
	Minimum gain	+4	dB
RX gain ripple	within 1 band	<1	dB
RX IIP3	High / low gain	-22 / +2	dBm
RX S_{11}	High gain	< -8	dB
LO frequencies		3.432 / 3.960 / 4.488	GHz
LO phase error	100Hz to 100MHz, band 1 / 2 / 3	1.5 / 1.7 / 1.9	deg RMS
LO hopping time	all 3 bands	<2	nsec
TX P_{1dB}	Max. gain	+5	dBm
TX EVM	@Pout up to -4dBm, band 1 / 2 / 3	-28 / -27.5 / -27	dB
Current consumption	RX chain @1.5V, w/o test buffer	34	mA
	TX chain @1.5V, @Pout of -4dBm	65	mA
	LO generation @1.5V	124	mA
Chip Area		6.6	mm^2
Technology	Infineon 0.13um standard digital CMOS, 1P6LM, MiM-Capacitors		

Figure 6.5.7: UWB transceiver performance summary.

